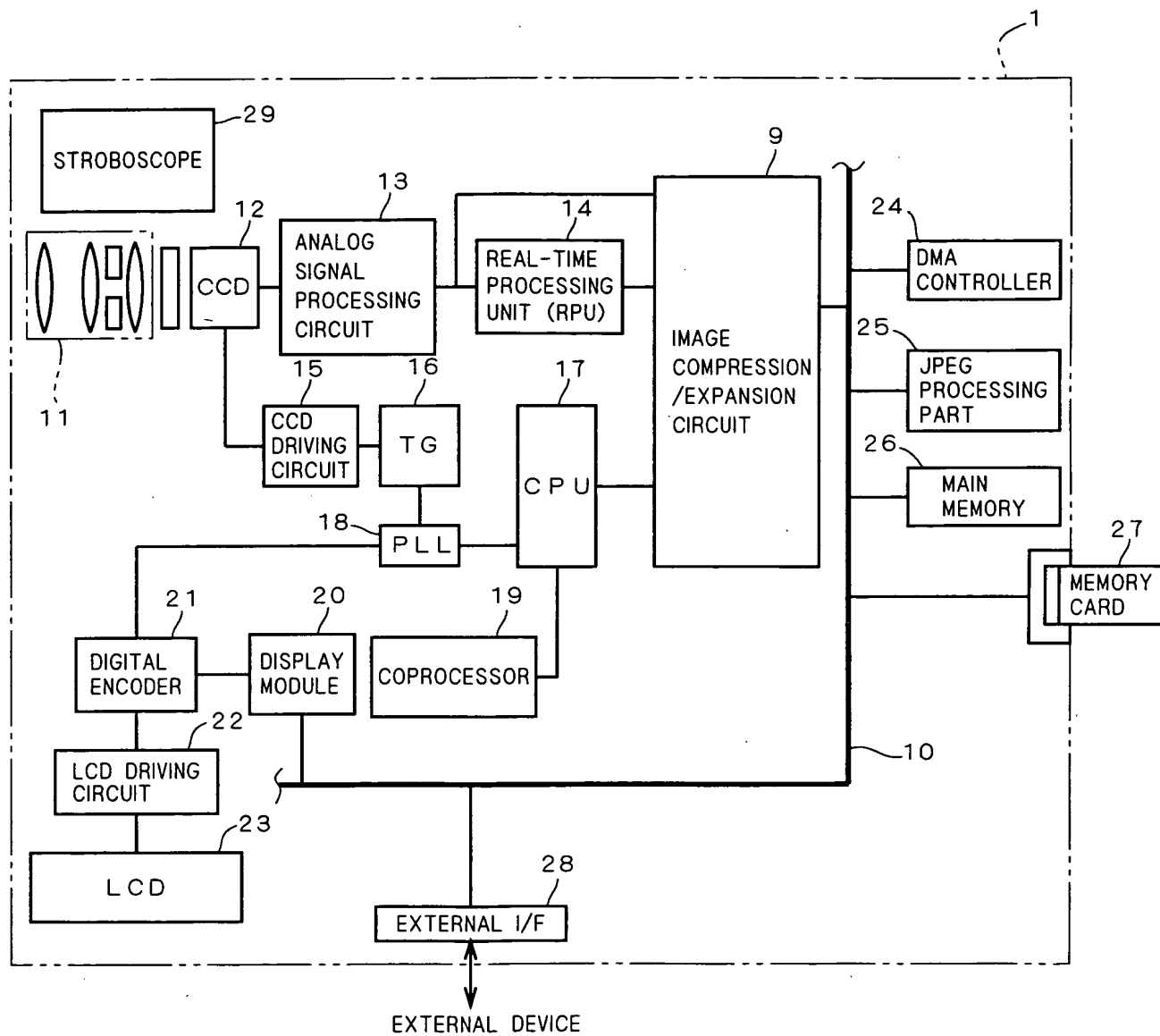
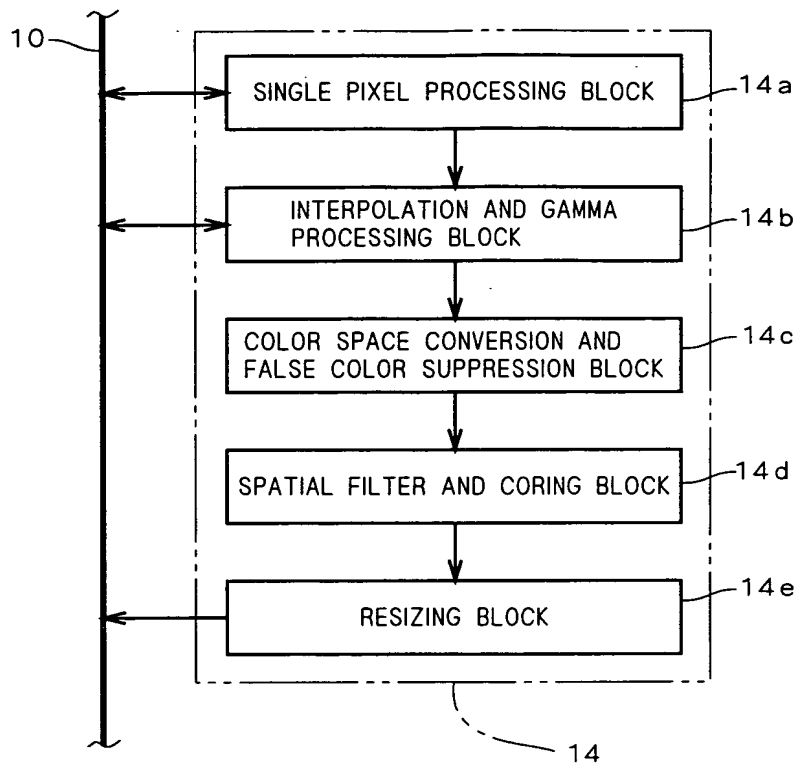


F I G . 1

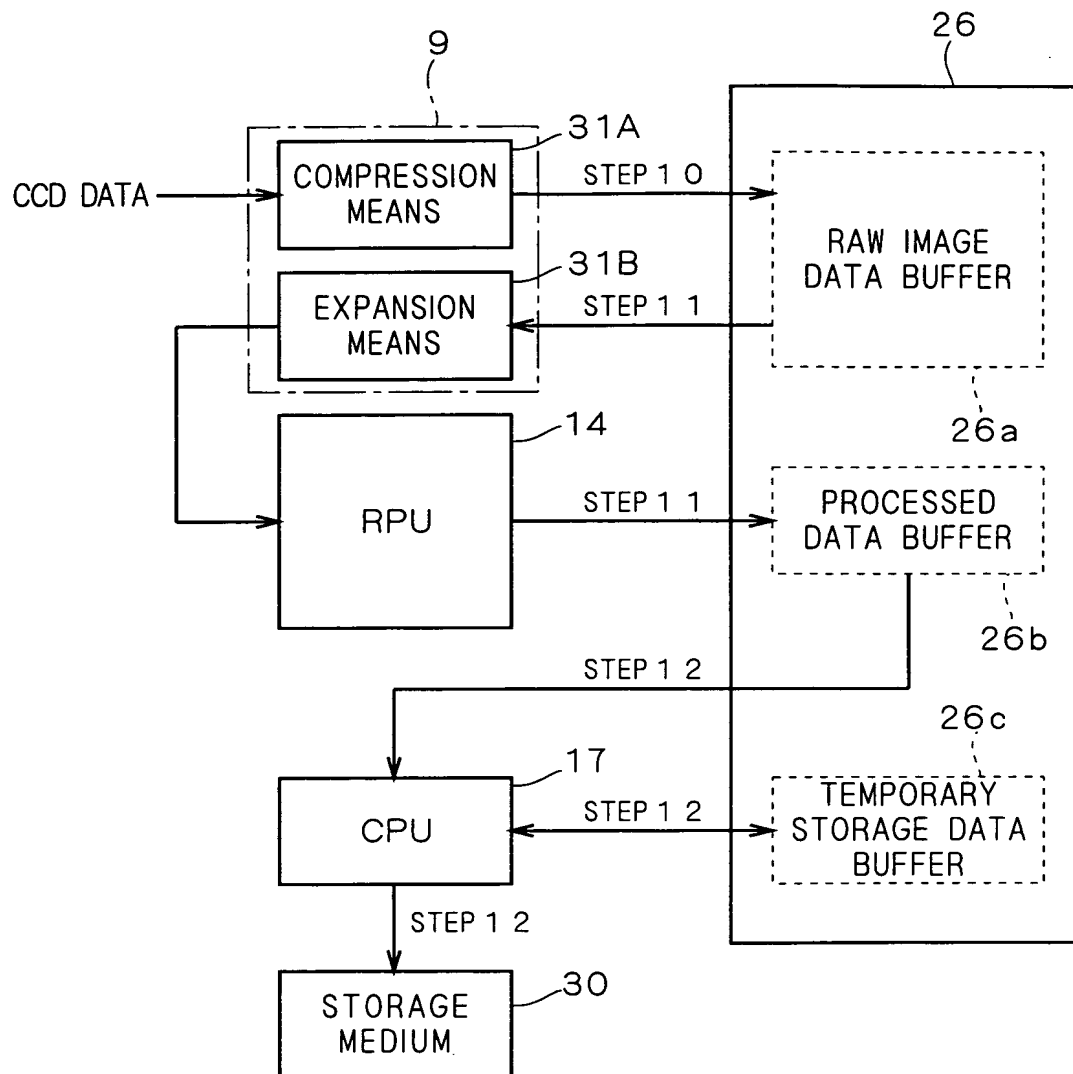


F I G . 2



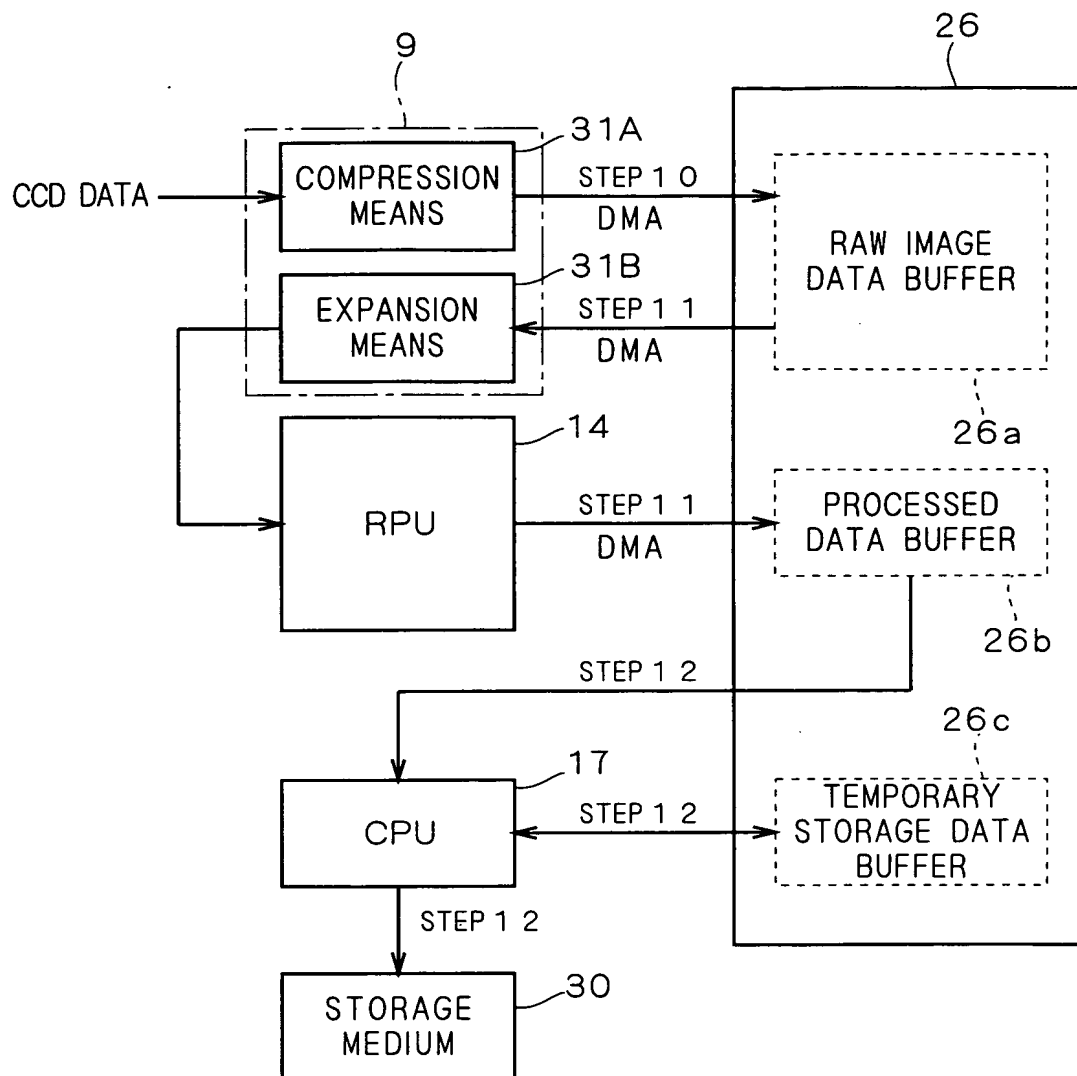
0394450" 05119660

F I G . 3



09964458.09601

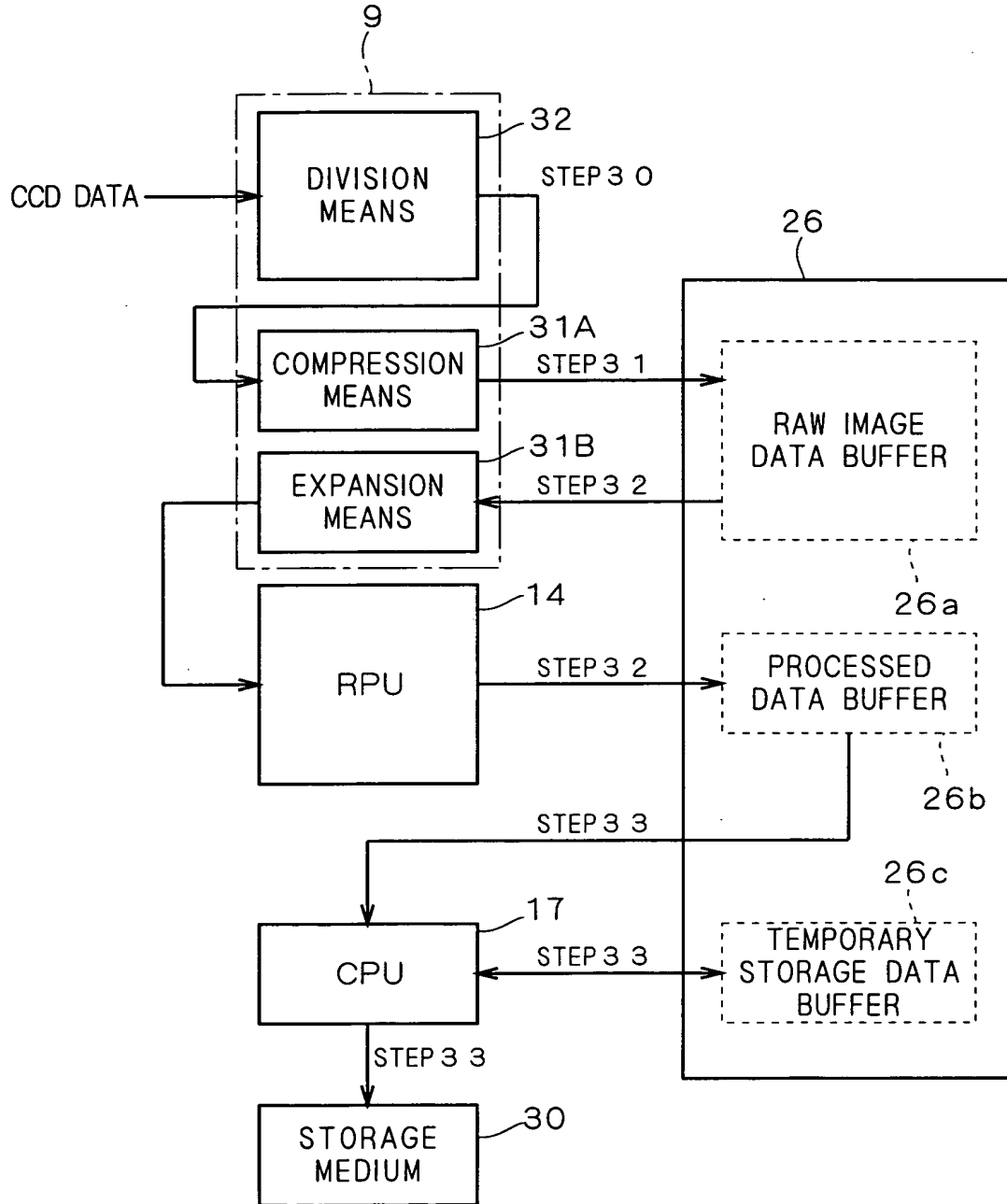
F I G . 4



09964453-092801

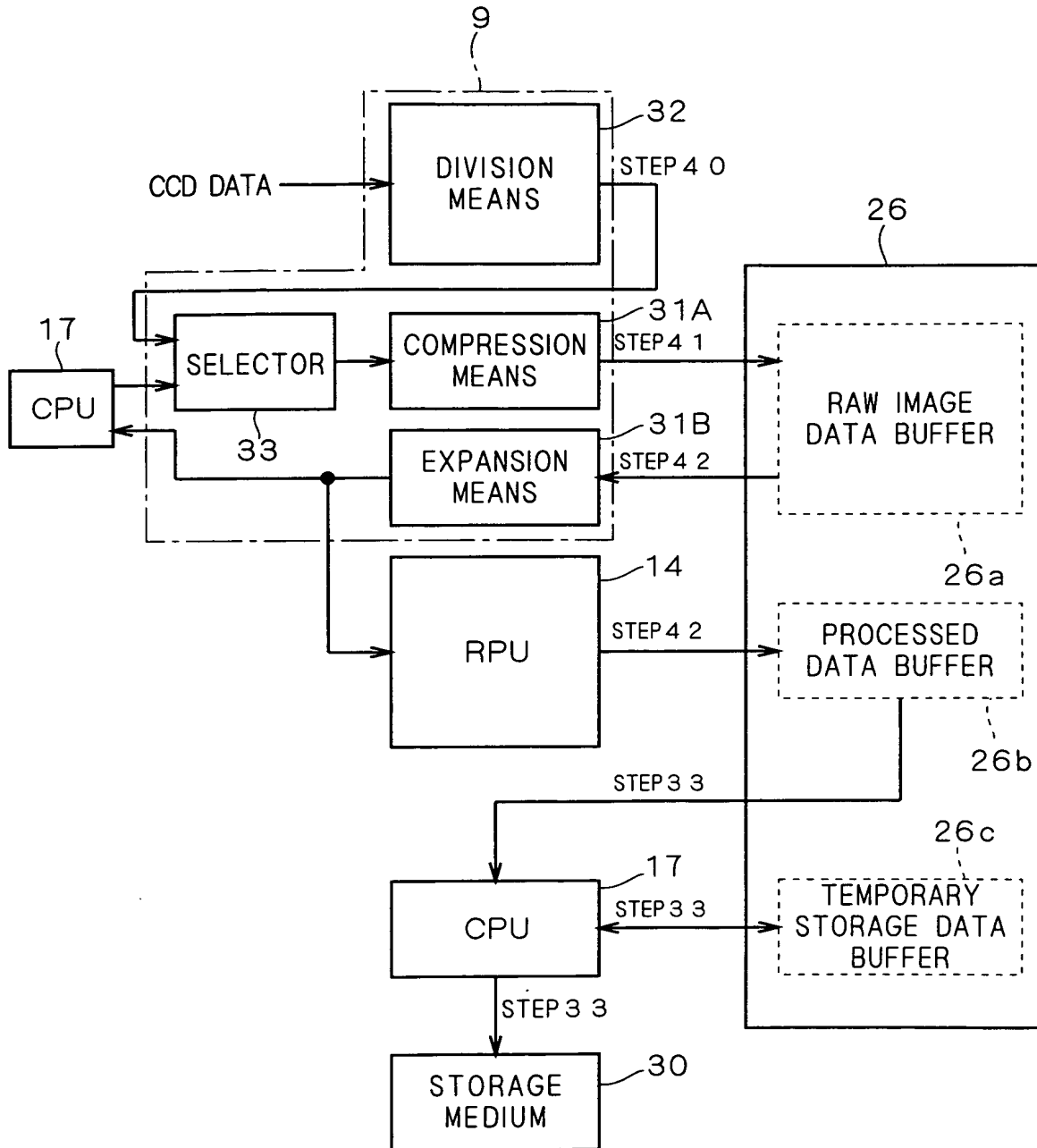
The block diagram illustrates the data processing system 26. It shows the flow of data from the CCD DATA input through the COMPRESSION MEANS (31A) and EXPANSION MEANS (31B) to the RPU (14). The RPU (14) is connected to the CPU (17) and the STORAGE MEDIUM (30). The system also includes a RAW IMAGE DATA BUFFER (26a), a PROCESSED DATA BUFFER (26b), and a TEMPORARY STORAGE DATA BUFFER (26c). Data flows are labeled with steps: STEP 2 0, STEP 2 1, and STEP 2 2. DMA (Direct Memory Access) is indicated for data transfer between the buffers and the RPU/CPU.

F I G . 6



096451-09201

F I G . 7



F I G . 8

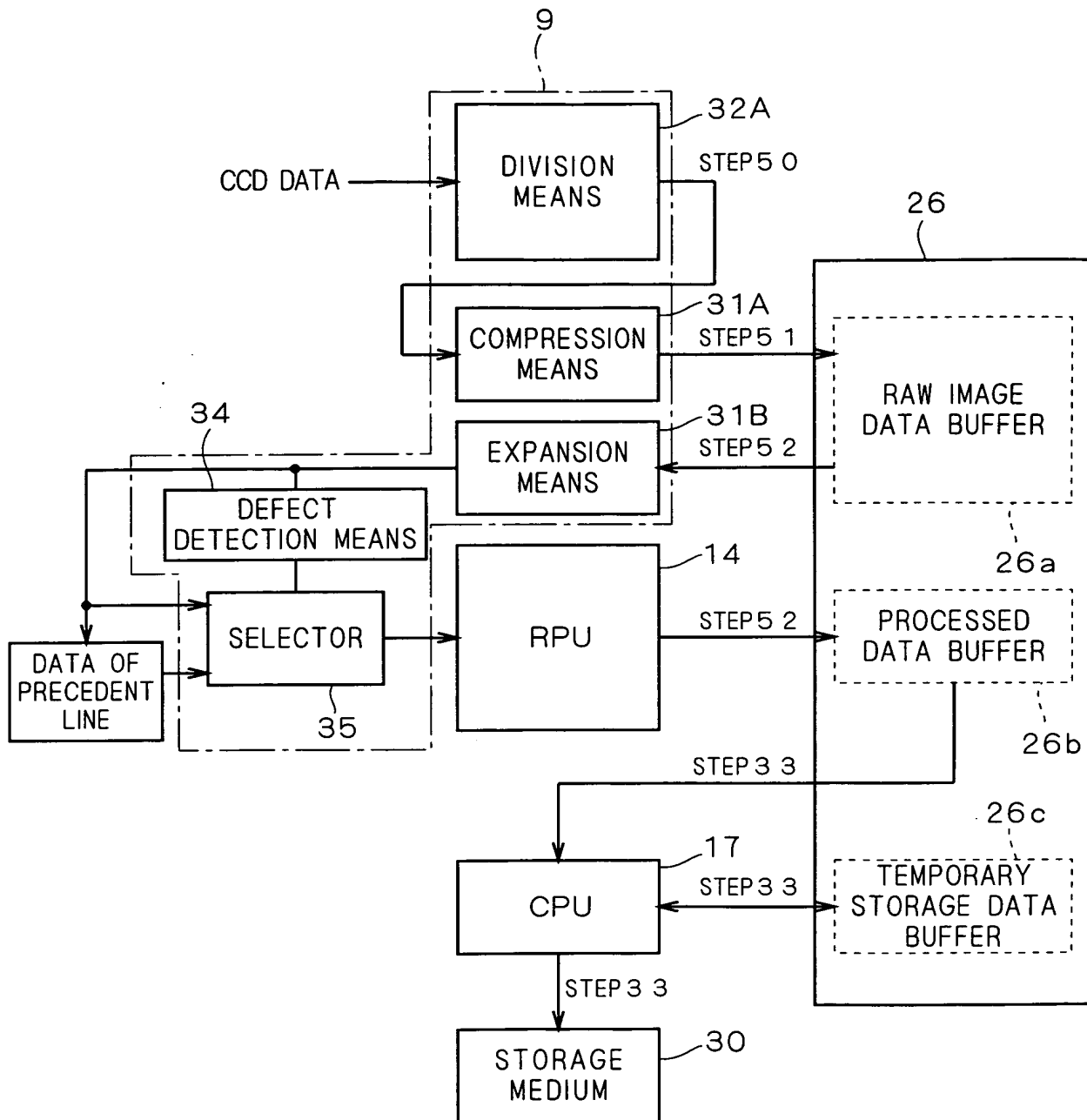
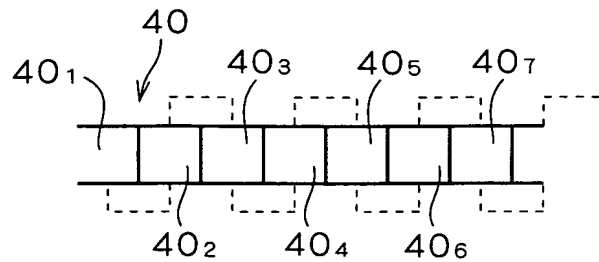


FIG. 8

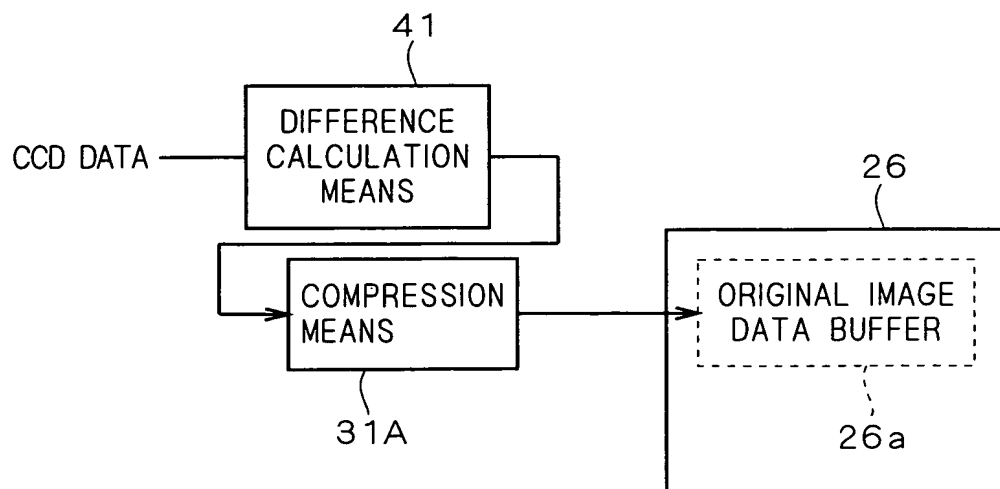


F I G . 9 A

CALCULATE DIFFERENCE BETWEEN ADJACENT PIXELS

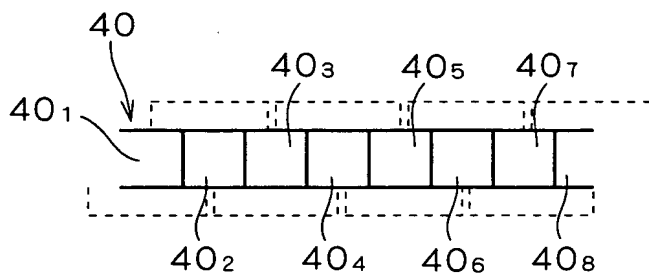


F I G . 9 B

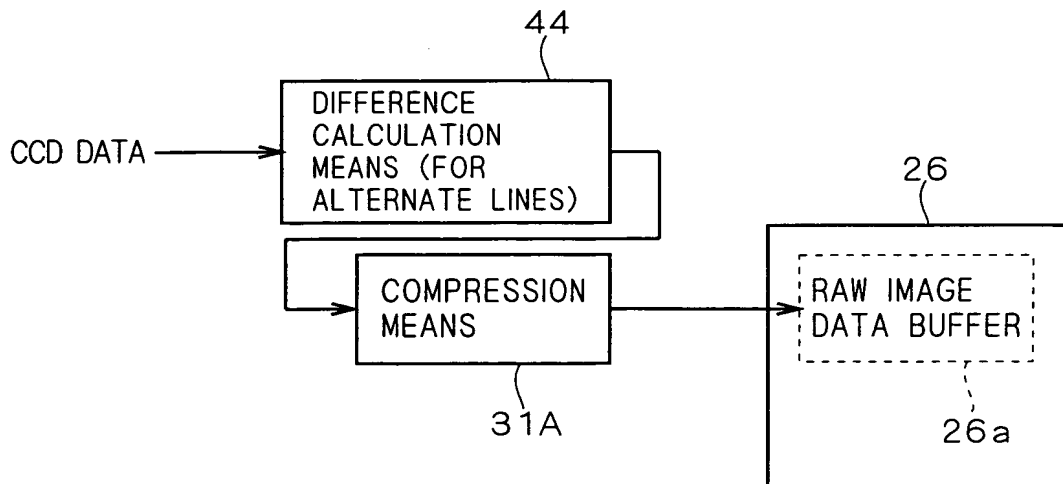


F I G . 1 0 A

CALCULATE DIFFERENCE BETWEEN ALTERNATE PIXELS

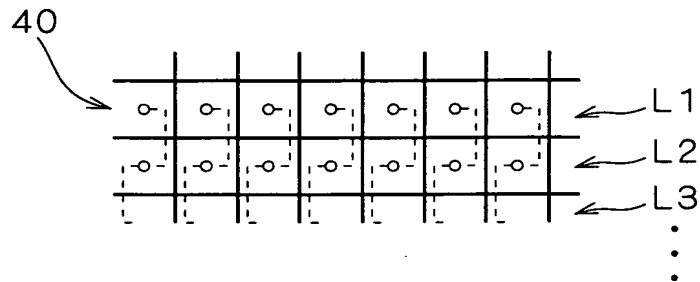


F I G . 1 0 B

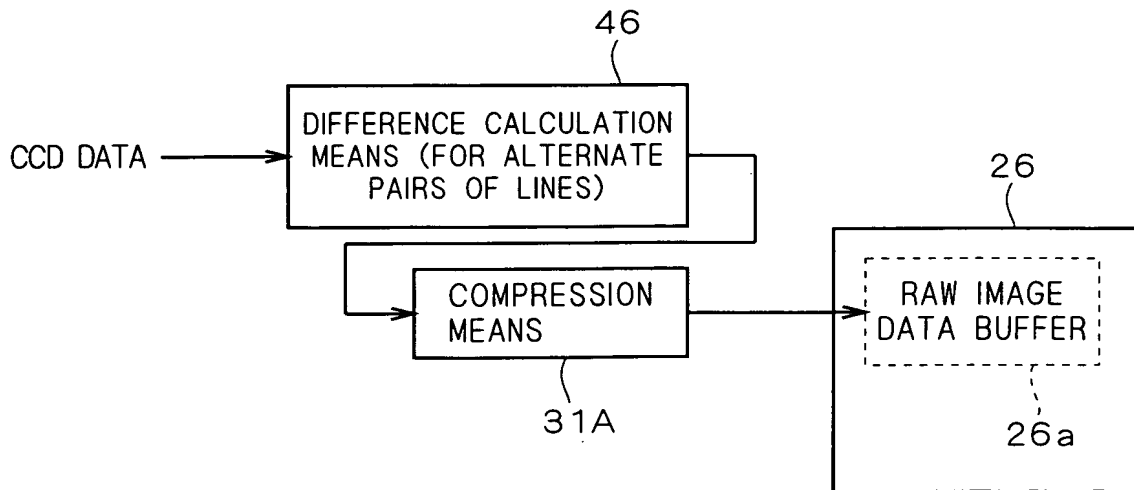


F I G . 1 1 A

CALCULATE DIFFERENCE BETWEEN VERTICAL PAIRS OF PIXELS  
ON ADJACENT PAIRS OF LINES

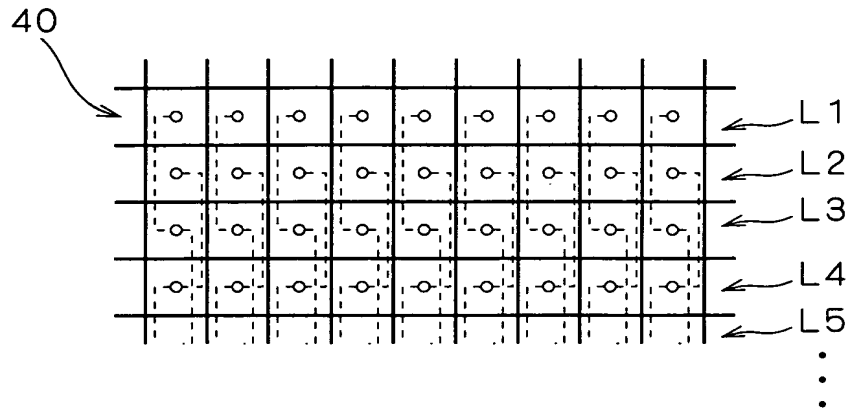


F I G . 1 1 B

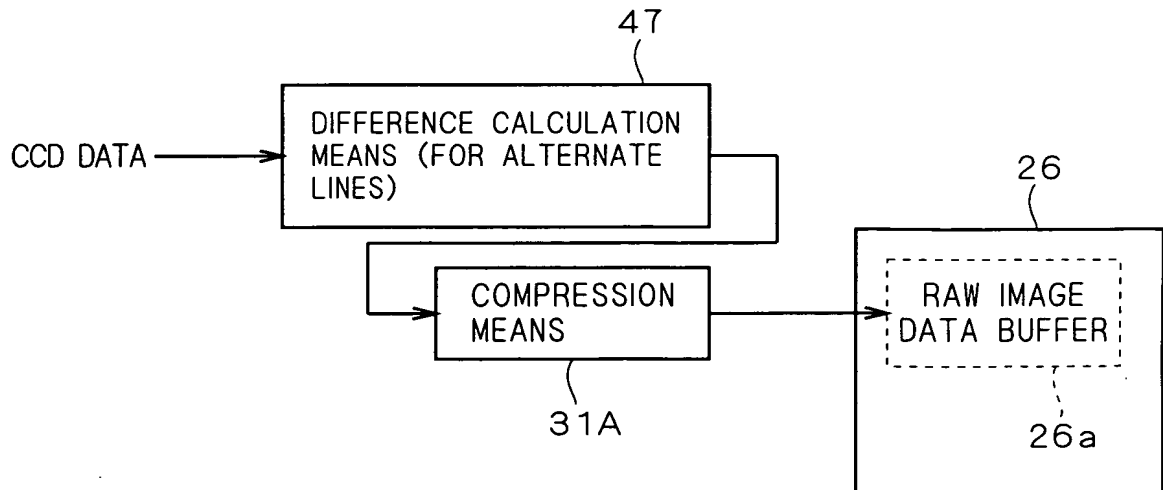


F I G . 1 2 A

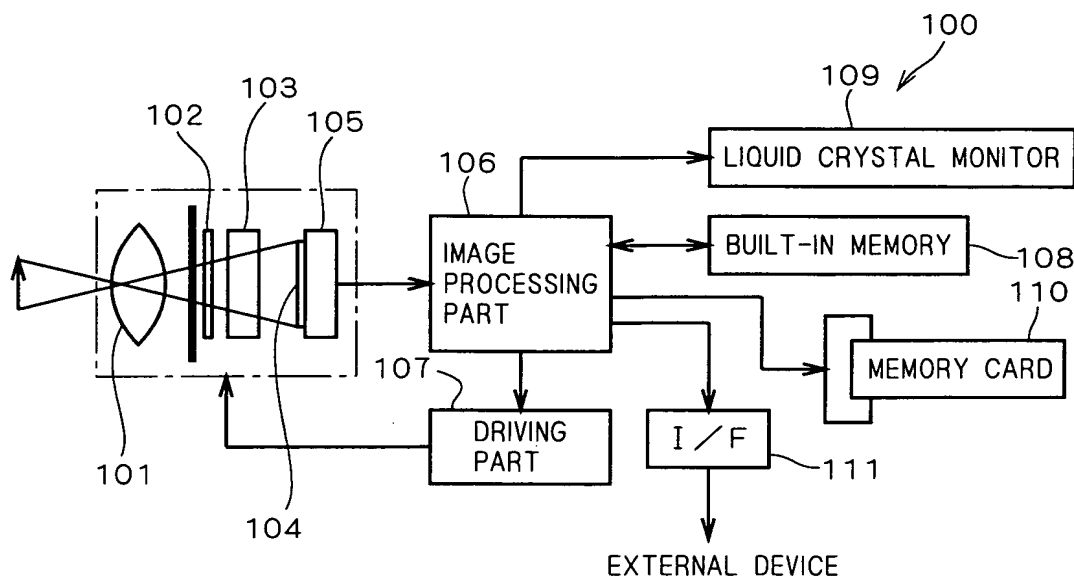
CALCULATE DIFFERENCE BETWEEN VERTICAL PAIRS OF PIXELS  
ON ALTERNATE PAIRS OF LINES



F I G . 1 2 B

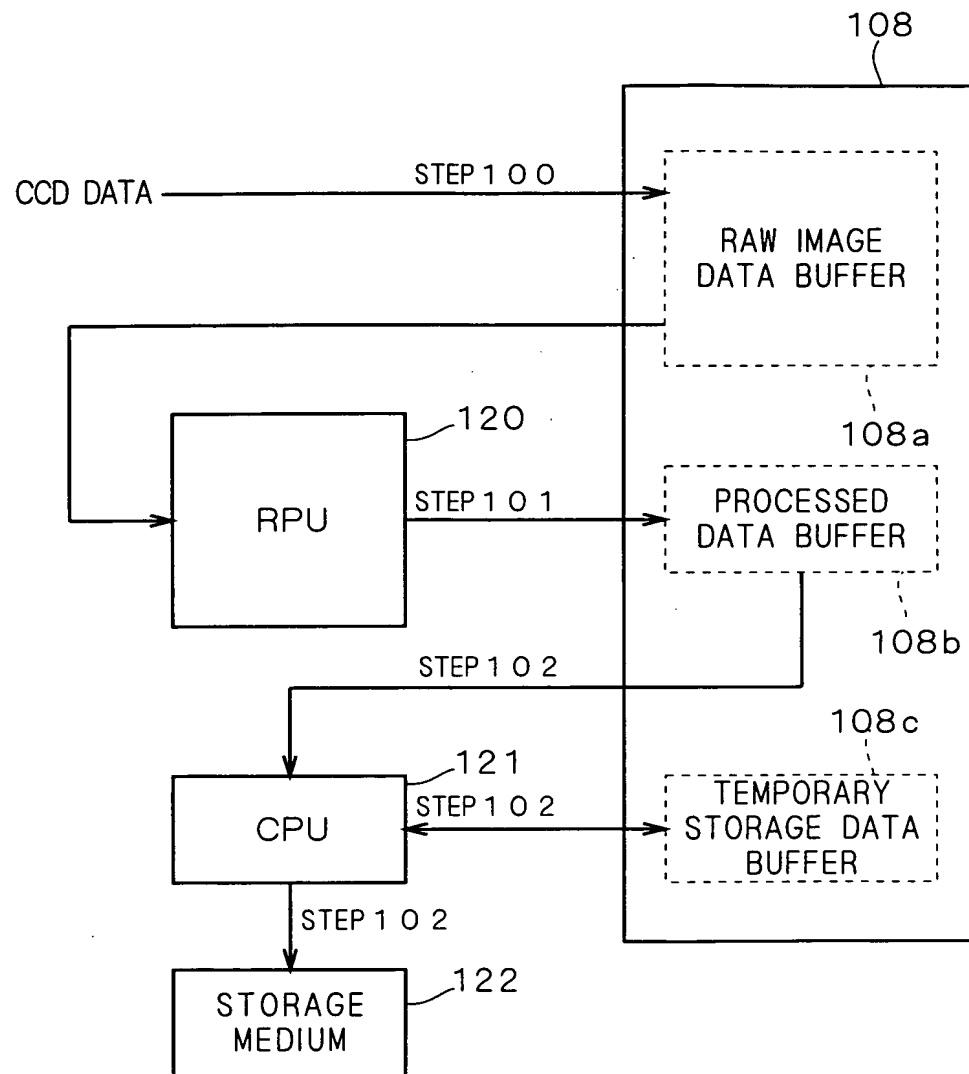


F I G . 1 3



096458.03201

F I G . 1 4



0964450 09660